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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,904	07/24/2003	Ritsuko Kawasaki	0756-7181	1203

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/625,904	KAWASAKI ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Minhloan Tran
Primary Examiner
Art Unit 2826

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/15/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. ("Yamazaki") JP 11-4001 in view of Chen USPN 5,965,916.

Yamazaki discloses in figs. 1-2 a semiconductor device comprising: a light-transmitting substrate 101; a base film 106 having a projection, the film being formed over one surface of the light-transmitting substrate; and an island-like semiconductor layer 107 having a crystal structure covering the projection and extending over a pair of edges of the projection, but lacks anticipation of a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film.

Chen discloses in fig. 6 a semiconductor device comprising a base film 3 having a projection; an island-like semiconductor layer 33; a gate insulating film 34 over an island-like layer; and a gate electrode 37 over the gate insulating film.

Therefore, in view of Chen's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki's device by incorporating a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film since that would minimize display flicker as taught by Chen.

4. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki in view of Chen.

Yamazāki discloses in figs. 1-2 a semiconductor device comprising: a light-transmitting substrate 101 and a thin film transistor over the light-transmitting substrate, wherein a base film 106 having a projection, the film being formed over one surface of the light-transmitting substrate; and an island-like semiconductor layer 107 comprising a channel formation region, at least a part of the channel formation region of the thin film transistor being provided over the projection and the island-like semiconductor layer covers the projection and extends over a pair of edges of the projection, but lacks anticipation of a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film.

Chen discloses in fig. 6 a semiconductor device comprising a base film 3 having a projection; an island-like semiconductor layer 33; a gate insulating film 34 over an island-like layer; and a gate electrode 37 over the gate insulating film.

Therefore, in view of Chen's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Yamazaki's device by incorporating a

gate insulating film over an island-like layer; and a gate electrode over the gate insulating film since that would minimize display flicker as taught by Chen.

As for claims 3 and 4, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

5. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeichi et al. ("Takeichi") USPN 6,258,723 in view of Chen.

Takeichi discloses in fig. 5 a semiconductor device comprising a light-transmitting substrate 20, a base film 22 having a region of a first thickness (under channel formation region) and a region of a second thickness (not under channel formation region) smaller than the first thickness, the film being formed over one surface of the light- transmitting substrate, and the region of the first thickness having an area smaller than the region of the second thickness; and an island-like semiconductor layer 23 having a crystal structure over the base film, the layer being formed over the region of the first thickness and the region of the second thickness, but lacks anticipation of a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film.

Chen discloses in fig. 6 a semiconductor device comprising a base film 3 having a projection; an island-like semiconductor layer 33; a gate insulating film 34 over an island-like layer; and a gate electrode 37 over the gate insulating film.

Therefore, in view of Chen's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Takeichi's device by incorporating a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film since that would minimize display flicker as taught by Chen.

6. Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeichi in view of Chen.

Takeichi discloses in fig. 5 a semiconductor device comprising: a light-transmitting substrate 20 and a thin film transistor over the light-transmitting substrate, wherein a base film 22 having a region of a first thickness (under channel formation region) and a region of a second thickness (not under channel formation region) smaller than the first thickness being provided over one surface of the light-transmitting substrate, the region of the first thickness has an area smaller than the region of the second thickness, at least a pad of a channel formation region of the thin film transistor being provided over the region of the first thickness, source and drain regions of the thin film transistor are provided over the projection and cover a pair of edges of the projection, and the island-like semiconductor, but lacks anticipation of a gate insulating film over an island-like layer; and a gate electrode over the gate insulating film.

Chen discloses in fig. 6 a semiconductor device comprising a base film 3 having a projection; an island-like semiconductor layer 33; a gate insulating film 34 over an island-like layer; and a gate electrode 37 over the gate insulating film.

Therefore, in view of Chen's teachings, one having an ordinary skill in the art at the time the invention was made would be motivated to modify Takeichi's device by incorporating a gate

insulating film over an island-like layer; and a gate electrode over the gate insulating film since that would minimize display flicker as taught by Chen.

As for the recitation that the island-like semiconductor layer is capable of being irradiated with light, it refers to an operational limitation and any such limitation must distinguish from the prior art in terms of structure rather than function, In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997); See also In re Swinehart, 439 F.2d210, 212-13, 169 USPQ 226, 228-29 (CCPA 1971; In re Danly, 263, F.2d 844, 847, 120 USPQ 528, 531 (CCPA 1959).

As for claims 13 and 14, the specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
August 22, 2005